# A 6-W *Ka*-Band Power Module Using MMIC Power Amplifiers

Daisy L. Ingram, *Member, IEEE*, D. Ian Stones, *Senior Member, IEEE*, Jeffrey H. Elliott, *Member, IEEE*, Huei Wang, *Senior Member, IEEE*, Richard Lai, and Michael Biedenbender, *Member, IEEE*

***Abstract*—This paper presents the development of a 6-W 24% power-added efficiency (PAE) $Ka$-band power module with an associated power gain of 21.5 dB. The power module consists of a driver amplifier and two power amplifier chips. These monolithic millimeter-wave integrated (MMIC) amplifiers were fabricated with a 2-mil-thick substrate using 0.15-$\mu$m InGaAs/AlGaAs/GaAs high electron mobility transistor (HEMT) technology. The driver amplifier is a fully matched single-ended design with an output power of 27.5 dBm, a 10.7-dB power gain and 27% PAE. We use a hybrid approach for the output power amplifier, which consists of two partially matched MMIC chips and an eight-way Wilkinson combiner fabricated on Alumina substrate. The MMIC power amplifiers delivered a record power of 35.4 dBm (3.5 W) with a PAE of 28% and an associated power gain of 11.5 dB. The eight-way combiner has an insertion loss of 0.6 dB.**

***Index Terms*— Millimeter wave transmitters, MMIC power amplifiers, MMIC transmitters, power dividers/combiners.**

## I. Introduction

LOW COST, light weight, high yield, and good reliability are the key parameters for the successful development of missile seekers, electronic warfare, smart munition, and the recent commercial point-to-point communication applications. With the maturing of the high electron mobility transistor (HEMT) technology, monolithic millimeter-wave integrated circuit (MMIC) power amplifiers offer all of the above benefits and have generated considerable interest in the power electronic community in the recent years. There have been numerous reports on the monolithic power amplifiers [1]–[8], with the best reported power at $Ka$-band of 1 W. This paper describes a new benchmark for the state-of-the-art performance achieved by a single MMIC chip and a module using these chips as building blocks, i.e., 6-W output power with 24% power-added efficiency (PAE) and 21.5-dB associated gain.

## II. Power HEMT Process

The frontside 0.15-$\mu$m HEMT process used for the $Ka$-band power MMIC's is the same as our previously reported high-yield V-band power MMIC production process [4] with the baseline double heterostructure $In_{0.22}Ga_{0.78}As$/AlGaAs/GaAs HEMT device profile as shown in Fig. 1. Using plasma enhanced chemical vapor deposition (PECVD) for device passivation, 175-nm silicon nitride is deposited. The key change in the process is the fabrication of the devices and circuits on a 2-mil-thick GaAs substrate compared with our previously reported 4-mil-thick GaAs substrate baseline [2], [5], [9], [12].

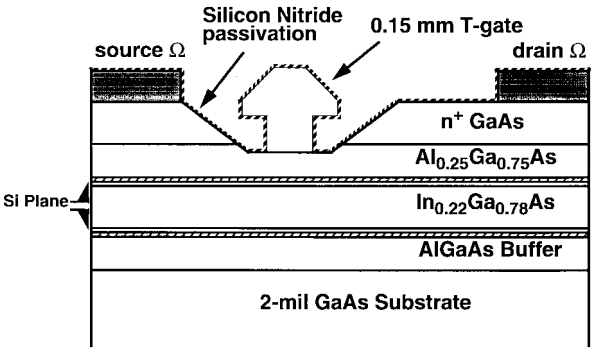


Fig. 1. Cross section of pseudomorphic double 0.15-$\mu$m InGaAs/AlGaAs/GaAs HEMT.

Recent development of the 2-mil GaAs HEMT fabrication technology has made it possible to pack more power within the same device periphery and provides a low-cost solution for a high-volume high-power system without sacrificing the state-of-the-art performance. The 2-mil-thick GaAs process has the advantages of providing a shorter thermal path and a smaller via hole pattern to the back side, thus allowing multiple via holes to be inserted between the gate fingers without increasing the pitch of the gate fingers. The multiple via holes to ground lowers the overall source inductance of the device, which results in improving the gain and PAE of the amplifier, especially at millimeter-wave frequency range. When more device cells are combined to provide higher output power, the source inductance advantage can be even more pronounced. These multiple vias to ground also decrease the thermal resistance of the device by as much as 30%, which results in a lower channel operating temperature [4]. Based on our past experience with 4-mil substrate designs, the power density delivered by the 2-mil device is at least 25%–35% better than the 4-mil device of similar periphery [1]–[4], [6], [7], [11], [12].

## III. Device Models

Statistically average linear and nonlinear device models were developed due to high volume production requirement for

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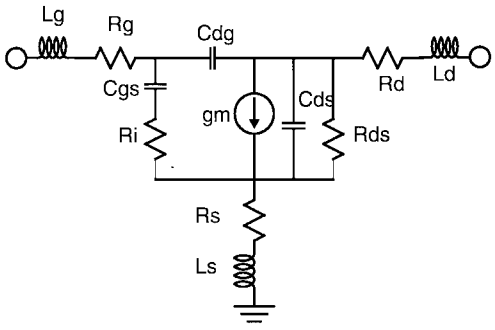
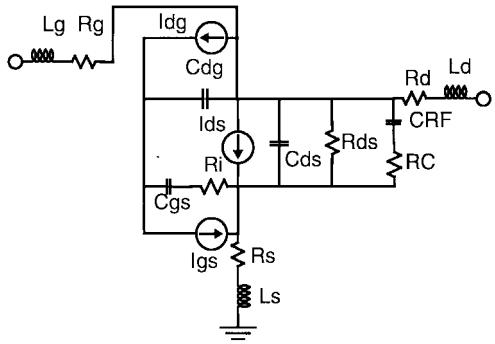



(a)

| Parameters | 500 μm device model | Parameters | 500 μm device model |
|---|---|---|---|
| Gm(S) | 0.263556 | Rg(ohm) | 1.3 |
| t(ps) | 1.584374 | Rd(ohm) | 0.579158 |
| Cgs(pF) | 0.554 | Rs(ohm) | 0.35 |
| Cdg(pF) | 0.032752 | Lg(nH) | 0.025 |
| Cds(pF) | 0.131385 | Ld(nH) | 0.01824 |
| Rds(ohm) | 90 | Ls(nH) | 0.00102 |
| Ri(ohm) | 0.878325 | | |

(b)

Fig. 2. (a) HEMT small signal model and (b) equivalent circuit parameters for 500 $\mu$m device at $V_{\rm ds} = 5$ V and 100% $I_{\rm ds}$ peak transconductance.




(a)

| Parameters | 500 μm device model | Parameters | 500 μm device model |
|---|---|---|---|
| A0 | 0.202 | Cgs(pF) | 0.554 |
| A1 | 0.231 | Cdg(pF) | 0.032752 |
| A2 | -0.069 | Cds(pF) | 0.131385 |
| A3 | -0.069 | VBI(V) | 0.75 |
| Beta | 0.018 | VTO(V) | -0.85 |
| Gamma | 2.3 | VDS0(V) | 5 |
| RDS0(ohm) | 275 | CRF(pF) | 1500 |
| RC(ohm) | 160 | RIN(ohm) | 0.878325 |
| TAU(ps) | 1.584374 | | |

(b)

Fig. 3. (a) Asymmetric Curtice nonlinear model and (b) equivalent nonlinear model parameters.

system insertion. Based on the TRW database, these models represent the average models over the process variation of 100-plus wafers. Extensive dc and RF measurements were done over different bias conditions at both active and cold

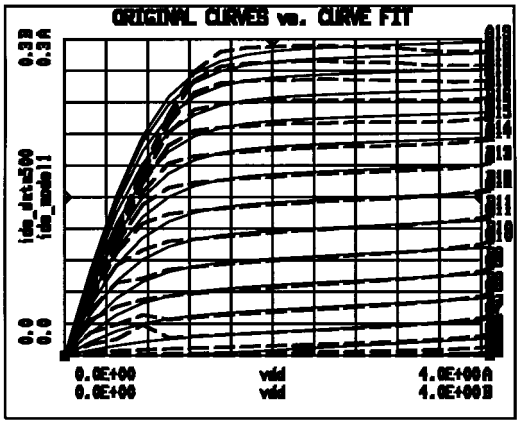



Fig. 4. DC–IV curve fit for the 500 $\mu$m device.

FET conditions [11] for different device sizes. Fig. 2 shows the linear hybrid-$\pi$ model for the 500-$\mu$m device and its circuit parameters. The asymmetric Curtice nonlinear model topology and the large signal model parameters for the 500-$\mu$m device are shown in Fig. 3. The pulsed DC–IV data were fitted by the asymmetric Curtice nonlinear model equations, as shown in Fig. 4. Verification of the nonlinear model was done by comparing the measured small signal $s$-parameters and power dependent $s$-parameters from the nonlinear model at the operating bias condition of the amplifier ($V_{\rm ds} = 5$ V and 50% $I_{\rm ds}$ at peak transconductance).

Fig. 5 shows the comparison of the small signal $s$-parameters and the power dependent $s$-parameters obtained from the nonlinear model at low power input at $V_{\rm ds} = 5$ V and 50% $I_{\rm ds}$ at peak transconductance. These models were extracted using microstrip device test structures to ensure that the device characterizations were done in the same microstrip propagation environment as they were used inside a circuit.

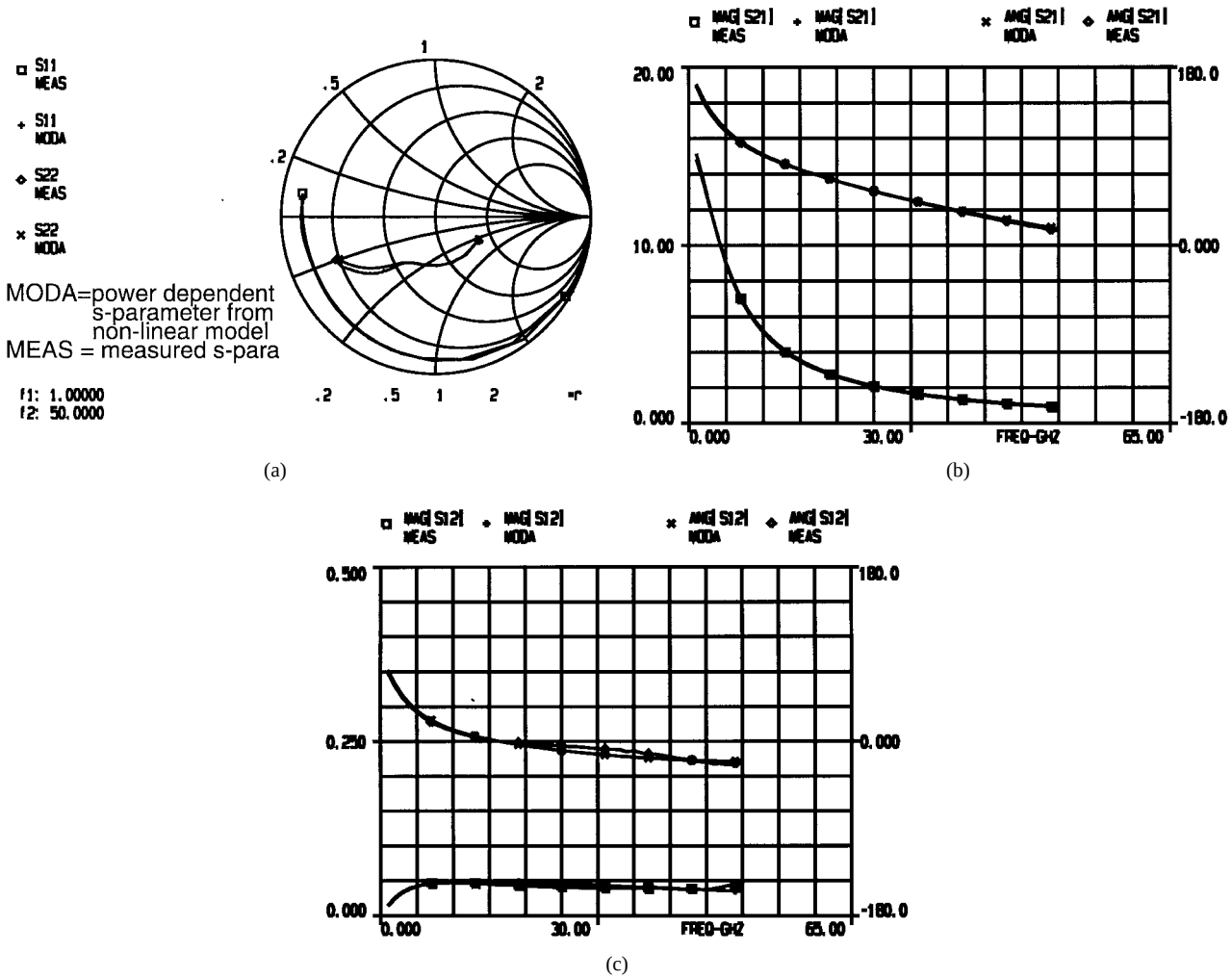
## IV. Circuit Design

### A. Driver Amplifier

Fig. 6 shows the photograph of the driver amplifier. The driver amplifier is a two-stage single-ended design with the output device periphery of 1.52 mm. Conservative device drive ratio was used to ensure enough power to drive the output stage over process variation. Harmonic terminations were provided at the drain to improve the PAE, and these also help the out-of-band stability. This chip was fully matched to 50 $\Omega$ at the input and output. Stability analysis was done on both stages to make sure there was sufficient margin over process variation. Odd mode clamping resistors were inserted between FET's to suppress the push–pull oscillation. Odd mode stability analysis was done according to [10]. Out-of-band oscillation was suppressed by resistively loaded quarter-wave stubs. The chip can be biased from either side for flexibility of insertion into different power modules. The chip area is 4.0 mm $\times$ 1.5 mm.

### B. Power Amplifier

Fig. 7 shows the photograph of the power amplifier. The output MMIC power amplifier is a two-stage single-ended




(a) (b) (c)

Fig. 5. (a) Verification of nonlinear model, (b) verification of nonlinear model, and (c) verification of nonlinear model.

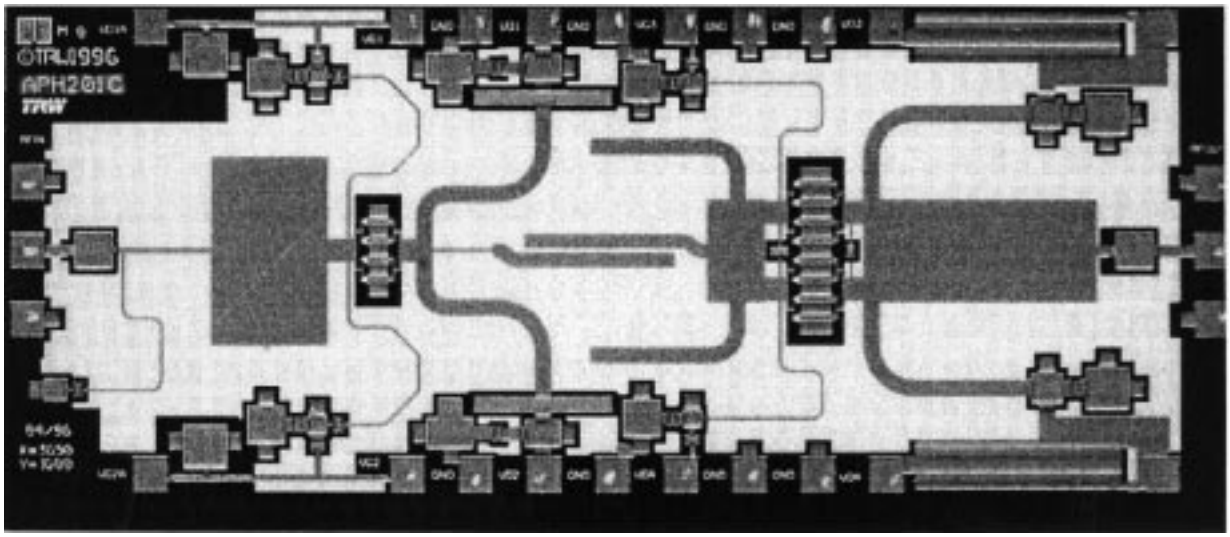



Fig. 6. Photograph of the driver amplifier MMIC chip (4.0 × 1.5 mm).

design with the output device periphery of 6.72 mm. optimum load at the fundamental and second harmonic were determined from the computer load pull of the nonlinear model using HPEE's of Libra simulator. Devices were biased at class AB at $V_{\rm ds} = 5$ V to achieve the optimal power and PAE combination. A wide transmission line was used to transform the device impedance to some intermediate impedance. Odd mode clamping resistors were inserted between FET's to

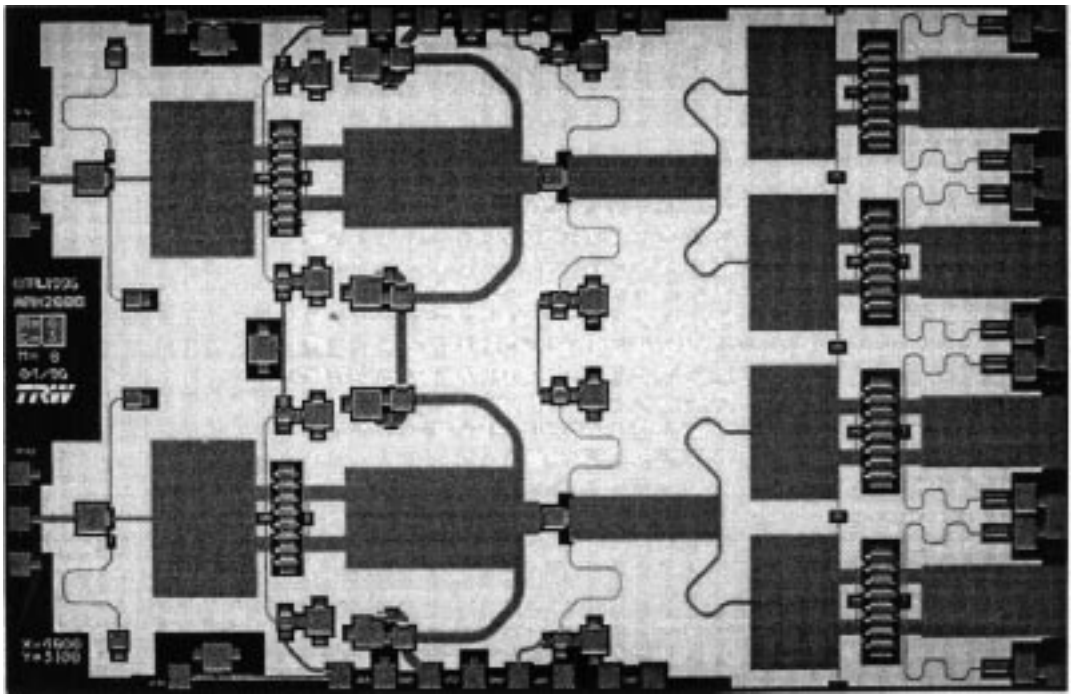


Fig. 7. Photograph of the power amplifier MMIC chip (4.8 × 3.1 mm).

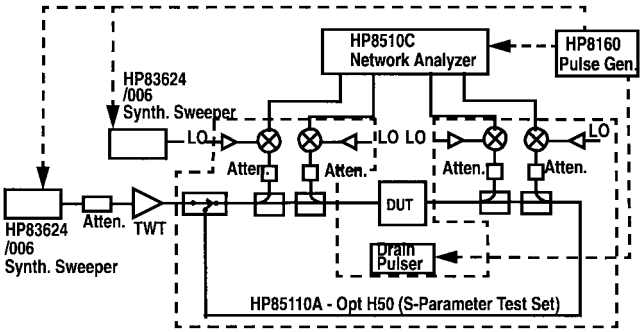



Fig. 8. Block diagram of on-wafer pulsed power test set.

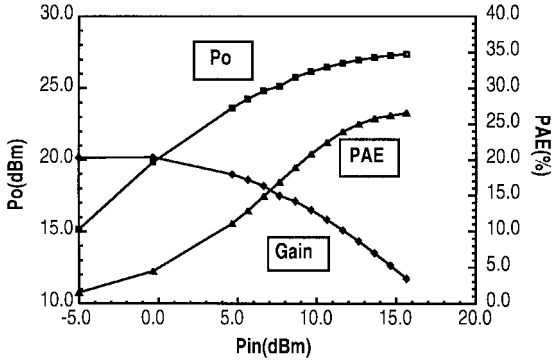



Fig. 9. Chip performance for MMIC driver amplifier at 34.5 GHz.

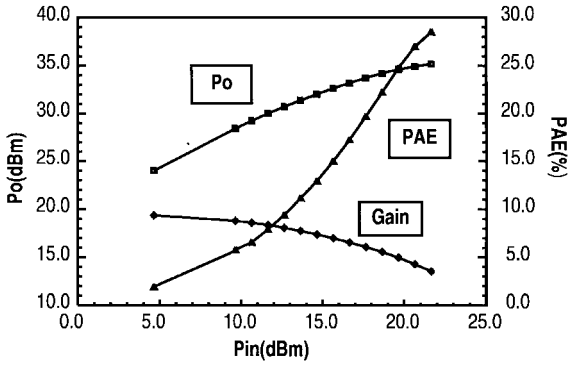



Fig. 10. Chip performance for MMIC power amplifier at 34.5 GHz.

suppress the push–pull oscillation. Harmonic terminations were provided at the drain to improve the PAE, and these also help the out-of-band stability. Out-of-band oscillation was suppressed by resistively loaded quarter-wave stubs. Drain bias currents are provided through the off-chip eight-way combiner. The layout of the chip is completely symmetrical to suppress any odd mode oscillation and the biases can be provided from either side of the chip. Based upon the capability of the TRW automated assembly line, the statistical average of the gap spacing was determined for the MMIC–MIC interface. This was simulated using a three-dimensional full-wave electromagnetic simulator, high frequency system simulator (HFSS), and the mismatch loss of the ribbon was compensated on the microwave integrated circuit side.

### *C. Wilkinson Combiners*

The output eight-way off-chip combiner consists of three tiers of Wilkinson binary combiners in microstrip configuration fabricated on Alumina substrate. The impedance level of the microstrip lines was chosen such as to give a wide line width. Hence, the dissipative transmission loss of the combiners was minimized. Each Wilkinson combiner was designed separately to operate between the chosen port impedance. It was modeled on either Sonnet or HFSS and simulated in order to obtain the frequency response. The arm line of each combiner was

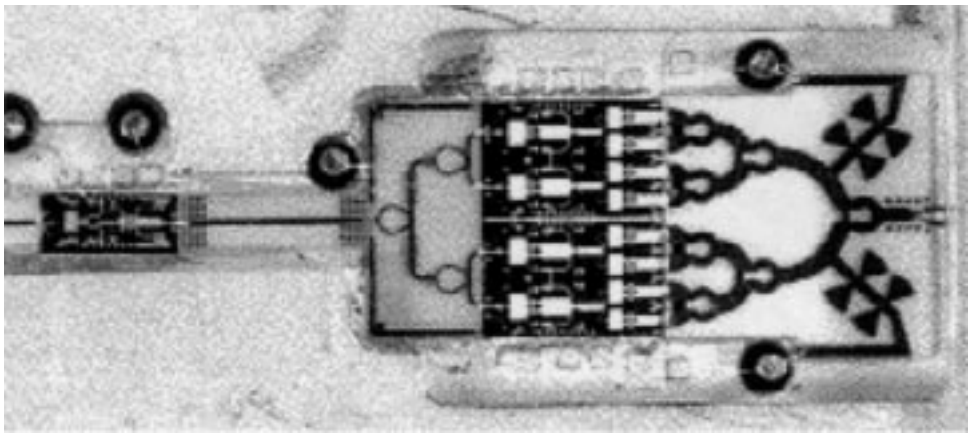


Fig. 11. Photograph of the 6-W power module.

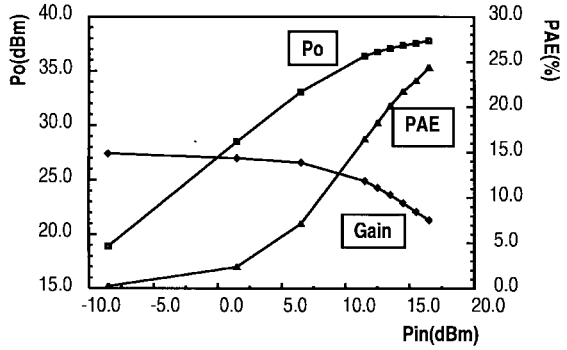



Fig. 12. Measured in-fixture performance of the 6-W power module.


Fig. 13. On-wafer pulsed power measurement of the driver amplifier.

then adjusted in length and width to obtain the best return loss and transmission loss. The combiner was fine-tuned for best input port match and port-to-port isolation. Due to the close proximity of the input ports, the final configuration had a simulated transmission unbalance of 0.3 dB and 8°. A bias feed was also designed on the combiner substrate. It was a three-section band stop filter. Its measured rejection at $Ka$-band was 35 dB. The combiner was measured in a back-to-back configuration. The measured loss of one combiner was 0.6 dB. The input combiner consists of two levels of Wilkinson corporate combiners and the measured loss of the combiner is 0.4 dB.

## V. On-Wafer Pulsed Power Test Set

Fig. 8 shows the block diagram of the TRW fully-automated on-wafer pulse power measurement test set. Both RF and dc drain current were pulsed with a pulse period of 2 $\mu$s at 0.5% duty cycle [2], [12], [13]. This test set performs on-wafer measurement of the "large signal" $s$-parameter, thus measuring the power performance of MMIC chips. This substantially reduces the time spent on fixture evaluation of the chips and allows pre-assembly dc and RF power screening of the chips once the correlation is established between on-wafer and fixture data. This will substantially reduce the cost of re-work in production due to power fall short of specifications. The short pulse duty cycle prevents excessive device heating during the on-wafer circuit measurement when no heat-sink is provided. This helps to bridge the gap between on-wafer measurement and fixture measurement discrepancy.

## VI. Measured Performance

Fig. 9 shows the measured power, power gain and the PAE of the driver amplifier at 34.5 GHz in a fixture. The PAE peaks at 27% with an output power of 27.5 dBm and an associated gain of 10.7 dB. The in-fixture measured data of the power amplifier at 34.5 GHz is shown in Fig. 10. The power amplifier demonstrated 35.4-dBm (3.5-W) saturated output power at 28% PAE with an associated power gain of 11.5 dB. This corresponds to a power density of over 550 mW/mm at the device level, which is about 28%–30% better than the recorded power density for its 4-mil counterpart [2] at $Ka$-band. Fig. 11 shows a photograph of the power module with one driver amplifier driving two power amplifiers. The four-way splitter has a measured loss of 0.4 dB and the eight-way combiner at the output has a measured loss of 0.6 dB. Fig. 12 shows the measured performance of the entire power module including its coaxial interfaces (K-connectors) with an output power of 37.8 dBm ($>$6 W), PAE of 24%, and an associated gain of 21.5 dB at 34.5 GHz. In comparison with the 4-mil power module system we published a few years ago, the 2-mil technology has allowed us to put together a 6-W power module with a total GaAs substrate real estate of 35.76

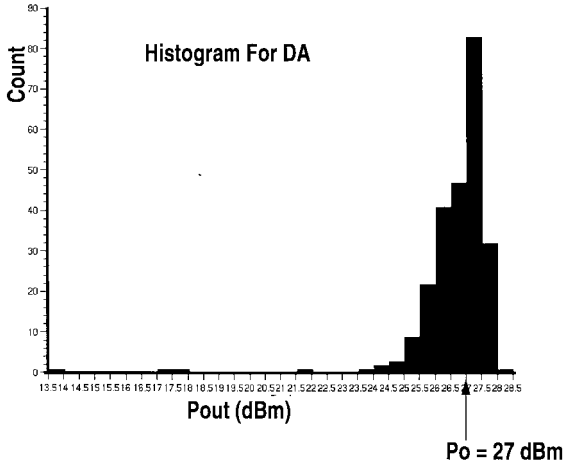



Fig. 14. Histogram for the driver amplifier.

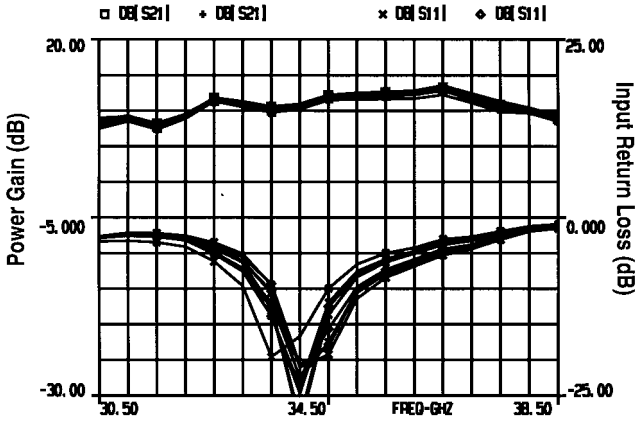



Fig. 15. On-wafer pulsed power measurement of the power amplifier.

mm$^2$ instead of the previously recorded 66.24 mm$^2$ (an 85% reduction). The chip count drops from six to three chips. This improvement significantly reduces the cost of assembly and production for a high-power module. Fig. 13 shows the on-wafer pulsed power measurement of the driver amplifier which produced an RF functional yield of 54% using power $>$27 dBm as screening criteria. Input return losses were better than 10 dB. The histogram of the drvier amplifier for 240 chips from four different wafers is shown in Fig. 14. The input power is 16 dBm and the mean is 27 dBm with a standard deviation of 0.79 dB. The fixture test data usually shows better power results than on-wafer test data by within 0.2–0.8 dB. The on-wafer pulsed power measurement of the power amplifier, which is shown in Fig. 15, produced an RF functional yield of 29% using $>$29 dBm per output port as screening criteria. The histogram of the power amplifier is shown in Fig. 16. The dip in gain shown in the passband of the on-wafer pulsed power measurement was due to the mismatch loss of the step discontinuity of the imperfect calibration standards created for the partially matched chip and did not show up in the fixture measurement.

## VII. Conclusion

A $Ka$-band power amplifier module consisting of three MMIC chips and capable of delivering 6-W output power with

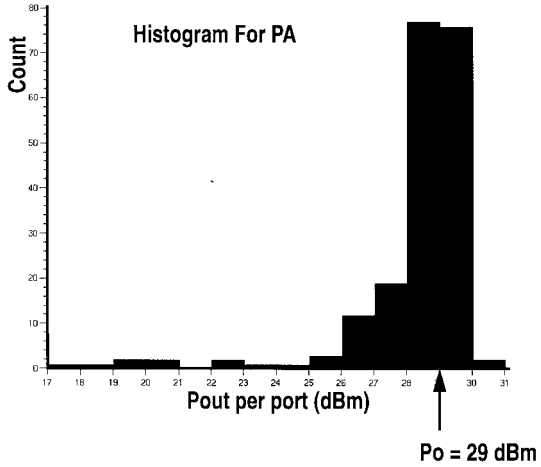



Fig. 16. Histogram for the power amplifier.

24% PAE and 21.5 dB associated gain was developed. The MMIC power amplifier chip, with 2-mil-thick substrate, has achieved 3.5-W output power at 28% PAE with an associated power gain of 11.5 dB.

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**Daisy L. Ingram** (M'97) received the B.S.E.E. and M.S.E.E. degrees from the University of California, Los Angeles, in 1984 and 1986, respectively. Her research was to design and construct a phase-locked loop system that stabilizes a 380-GHz submillimeter-wave carcinotron for a plasma diagnostic system.

She joined the Electronic Instrumentation Division, Eaton Corporation, in 1986, and became a key member of the microwave synthesizer and noise-gain analyzer teams, responsible for various signal processing and receiver component and module designs. She became a Staff Engineer for Rockwell International in 1991 and was the responsible Unit Engineer for the master frequency generator for the Extended Range Intercept-1 Technology (ERINT) missile program. From 1992 to 1994, she was with Hughes Torrance Research Center and was engaged in millimeter-wave MMIC component designs and HBT and InP HEMT device modeling. Since joining the RF Products Center, TRW, Inc., Redondo Beach, CA, in 1995, her main focus has been developing high-isolation and high-power Ka- to W-band MMIC components and modules, as well as HEMT and InP HEMT device modeling. She is currently a Department Staff Engineer and her present assignments are as IR&D Principal Investigator and Subproject Program Manager of the DARPA MAFET Thrust 3 program, developing W-band quasioptical power combining system.

Ms. Ingram is a member of Tau Beta Pi.

**D. Ian Stones** (M'72–SM'86) was born in Scunthorpe, England, U.K., in 1940. He received the B.Eng. degree from Sheffield University, U.K., in 1962 and the M.S.E.E. degree from California State University, Long Beach, CA in 1976. He has done postgraduate study at the University of Southern California, Los Angeles, CA.

From 1962 to 1964 he was with G.&E. Bradley, Ltd., Neasden, England, U.K.; from 1964 to 1968 he was with Ether Engineering, Ltd., Bushey, England, U.K.; from 1968 to 1971 he was with Anzac Electronics, Waltham, MA; and from 1971 to 1973 he was with Wavecom, Inc., Northridge, CA, where he designed filters and couplers. Since 1973, he has been with TRW, Inc., Redondo Beach, CA. He is presently a Technical Specialist and has been responsible for the development of passive linear components in the microwave and millimeter-wave frequency bands. In particular, he has designed coaxial and waveguide wideband high-power radial combiners suitable for high-order amplifier combining. He has also developed phase shifters, couplers, filters, and rotary transformers. Presently, he is involved in the design of low-loss transitions and spatial combiners.

**Jeffrey H. Elliott** (M'84), for a biography, see this issue, p. 2423.

**Huei Wang** (S'83–M'83–SM'95), for a photograph and biography, see this issue, p. 2423.

**Richard Lai**, for a photograph and biography, see this issue, p. 2423.

**Michael Biedenbender** (S'84–M'90), for a biography, see this issue, p. 2423.